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KEY=BOOK - LEON DESHAWN

THE CACHE MEMORY BOOK

Morgan Kaufmann **The Second Edition of The Cache Memory Book introduces systems designers to the concepts behind cache design. The book teaches the basic cache concepts and more exotic techniques. It leads readers through someof the most intricate protocols used in complex multiprocessor caches. Written in an accessible, informal style, this text demystifies cache memory design by translating cache concepts and jargon into practical methodologies and real-life examples. It also provides adequate detail to serve as a reference book for ongoing work in cache memory design. The Second Edition includes an updated and expanded glossary of cache memory terms and buzzwords. The book provides**

new real world applications of cache memory design and a new chapter on cache"tricks". Illustrates detailed example designs of caches Provides numerous examples in the form of block diagrams, timing waveforms, state tables, and code traces Defines and discusses more than 240 cache specific buzzwords, comparing in detail the relative merits of different design methodologies Includes an extensive glossary, complete with clear definitions, synonyms, and references to the appropriate text discussions

A PRIMER ON MEMORY CONSISTENCY AND CACHE COHERENCE

Morgan & Claypool Publishers **Many modern computer systems and most multicore chips (chip multiprocessors) support shared memory in hardware. In a shared memory system, each of the processor cores may read and write to a single shared address space. For a shared memory machine, the memory consistency model defines the architecturally visible behavior of its memory system. Consistency definitions provide rules about loads and stores (or memory reads and writes) and how they act upon memory. As part of supporting a memory consistency model, many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up-to-date. The goal of this primer is to provide readers with a basic understanding of consistency and coherence. This understanding includes both the issues that must be solved as well as a variety of solutions. We present both highlevel concepts as well as specific, concrete examples from real-world systems. Table of Contents: Preface / Introduction to Consistency and Coherence / Coherence Basics / Memory Consistency Motivation and Sequential Consistency / Total Store Order and the x86 Memory Model / Relaxed Memory Consistency / Coherence Protocols / Snooping Coherence Protocols / Directory Coherence Protocols / Advanced Topics in Coherence / Author Biographies**

A PRIMER ON MEMORY CONSISTENCY AND CACHE COHERENCE, SECOND EDITION

Springer Nature **Many modern computer systems, including homogeneous and heterogeneous architectures, support shared memory in hardware. In a shared memory system, each of the processor cores may read and write to a single shared address space. For a shared memory machine, the memory consistency model defines the architecturally visible behavior of its memory system. Consistency definitions provide rules about loads and stores (or memory reads and writes) and how they act upon memory. As part of supporting a memory consistency model, many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up-to-date. The goal of this primer is to provide readers with a basic understanding of consistency and coherence. This understanding includes**

both the issues that must be solved as well as a variety of solutions. We present both high-level concepts as well as specific, concrete examples from real-world systems. This second edition reflects a decade of advancements since the first edition and includes, among other more modest changes, two new chapters: one on consistency and coherence for non-CPU accelerators (with a focus on GPUs) and one that points to formal work and tools on consistency and coherence.

MULTI-CORE CACHE HIERARCHIES

Morgan & Claypool Publishers **A key determinant of overall system performance and power dissipation is the cache hierarchy since access to off-chip memory consumes many more cycles and energy than on-chip accesses. In addition, multi-core processors are expected to place ever higher bandwidth demands on the memory system. All these issues make it important to avoid off-chip memory access by improving the efficiency of the on-chip cache. Future multi-core processors will have many large cache banks connected by a network and shared by many cores. Hence, many important problems must be solved: cache resources must be allocated across many cores, data must be placed in cache banks that are near the accessing core, and the most important data must be identified for retention. Finally, difficulties in scaling existing technologies require adapting to and exploiting new technology constraints. The book attempts a synthesis of recent cache research that has focused on innovations for multi-core processors. It is an excellent starting point for early-stage graduate students, researchers, and practitioners who wish to understand the landscape of recent cache research. The book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI engineers. Table of Contents: Basic Elements of Large Cache Design / Organizing Data in CMP Last Level Caches / Policies Impacting Cache Hit Rates / Interconnection Networks within Large Caches / Technology / Concluding Remarks**

PROCESSOR MICROARCHITECTURE

AN IMPLEMENTATION PERSPECTIVE

Morgan & Claypool Publishers **This lecture presents a study of the microarchitecture of contemporary microprocessors. The focus is on implementation aspects, with discussions on their implications in terms of performance, power, and cost of state-of-the-art designs. The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories. Then, it describes the implementation of the fetch unit, where**

special emphasis is made on the required support for branch prediction. The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions. The next chapter presents the allocation stage and pays special attention to the implementation of register renaming. Afterward, the issue stage is studied. Here, the logic to implement out-of-order issue for both memory and non-memory instructions is thoroughly described. The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors, as well as the implementation of the bypass network, which has an important impact on the performance. Finally, the lecture concludes with the commit stage, where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations. This lecture is intended for an advanced course on computer architecture, suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture. It is also intended for practitioners in the industry in the area of microprocessor design. The book assumes that the reader is familiar with the main concepts regarding pipelining, out-of-order execution, cache memories, and virtual memory. Table of Contents: Introduction / Caches / The Instruction Fetch Unit / Decode / Allocation / The Issue Stage / Execute / The Commit Stage / References / Author Biographies

MEMORY SYSTEMS

CACHE, DRAM, DISK

Morgan Kaufmann **Is your memory hierarchy stopping your microprocessor from performing at the high level it should be? Memory Systems: Cache, DRAM, Disk shows you how to resolve this problem. The book tells you everything you need to know about the logical design and operation, physical design and operation, performance characteristics and resulting design trade-offs, and the energy consumption of modern memory hierarchies. You learn how to to tackle the challenging optimization problems that result from the side-effects that can appear at any point in the entire hierarchy. As a result you will be able to design and emulate the entire memory hierarchy. Understand all levels of the system hierarchy -Xcache, DRAM, and disk. Evaluate the system-level effects of all design choices. Model performance and energy consumption for each component in the memory hierarchy.**

SYSTEM PERFORMANCE TUNING

O'Reilly Media **Introduction to system performance; Monitoring system activity; Managing the workload; Memory performance; Disk performance issues; Network performance; Terminal performance; Kernel configuration.**

DESIGNING EMBEDDED HARDWARE

"*O'Reilly Media, Inc.*" **Intelligent readers who want to build their own embedded computer systems-- installed in everything from cell phones to cars to handheld organizers to refrigerators-- will find this book to be the most in-depth, practical, and up-to-date guide on the market. Designing Embedded Hardware carefully steers between the practical and philosophical aspects, so developers can both create their own devices and gadgets and customize and extend off-the-shelf systems. There are hundreds of books to choose from if you need to learn programming, but only a few are available if you want to learn to create hardware. Designing Embedded Hardware provides software and hardware engineers with no prior experience in embedded systems with the necessary conceptual and design building blocks to understand the architectures of embedded systems. Written to provide the depth of coverage and real-world examples developers need, Designing Embedded Hardware also provides a road-map to the pitfalls and traps to avoid in designing embedded systems. Designing Embedded Hardware covers such essential topics as: The principles of developing computer hardware Core hardware designs Assembly language concepts Parallel I/O Analog-digital conversion Timers (internal and external) UART Serial Peripheral Interface Inter-Integrated Circuit Bus Controller Area Network (CAN) Data Converter Interface (DCI) Low-power operation This invaluable and eminently useful book gives you the practical tools and skills to develop, build, and program your own application-specific computers.**

OPERATING SYSTEM, 2ND EDITION

Vikas Publishing House **The book Operating System by Rohit Khurana is an insightful work that elaborates on fundamentals as well as advanced topics of the discipline. It offers an in-depth coverage of concepts, design and functions of an operating system irrespective of the hardware used. With illustrations and examples the aim is to make the subject crystal clear and the book extremely student-friendly. The book caters to undergraduate students of most Indian universities, who would find subject matter highly informative and enriching. Tailored as a guide for self-paced learning, it equips budding system programmers with the right knowledge and expertise. The book has been revised to keep pace with the latest technology and constantly revising syllabuses. Thus, this edition has become more comprehensive with the inclusion of several new topics. In addition, certain sections of the book have been thoroughly revised. Key Features • Case studies of Unix, Linux and Windows to put theory concepts into practice • A crisp summary for recapitulation with each chapter • A glossary of technical terms • Insightful questions and model test papers to prepare for the examinations New in this Edition • More types of operating system, like PC and mobile;**

Methods used for communication in client-server systems. • New topics like: Thread library; Thread scheduling; Principles of concurrency, Precedence graph, Concurrency conditions and Sleeping barber problem; Structure of page tables, Demand segmentation and Cache memory organization; STREAMS; Disk attachment, Stable and tertiary storage, Record blocking and File sharing; Goals and principles of protection, Access control matrix, Revocation of access rights, Cryptography, Trusted systems, and Firewalls.

COMPUTER PROGRAMMING AND ARCHITECTURE

THE VAX

Digital Press **Takes a unique systems approach to programming and architecture of the VAX Using the VAX as a detailed example, the first half of this book offers a complete course in assembly language programming. The second describes higher-level systems issues in computer architecture. Highlights include the VAX assembler and debugger, other modern architectures such as RISCs, multiprocessing and parallel computing, microprogramming, caches and translation buffers, and an appendix on the Berkeley UNIX assembler.**

CORE MEMORY

A VISUAL SURVEY OF VINTAGE COMPUTERS

Chronicle Books **A stunning array of full-color photographs captures the history of modern technology through images of the computer collection of the Computer History Museum in Silicon Valley, offering revealing glimpses of such seminal machines as the Eniac, Crays 1-3, and Apple I and II, while describing each model, their innovations, and place in computer history.**

UNDERSTANDING THE LINUX KERNEL

"*O'Reilly Media, Inc.*" **To thoroughly understand what makes Linux tick and why it's so efficient, you need to delve deep into the heart of the operating system--into the Linux kernel itself. The kernel is Linux--in the case of the Linux operating system, it's the only bit of software to which the term "Linux" applies. The kernel handles all the requests or completed I/O operations and determines which programs will share its processing time, and in what order. Responsible for the sophisticated memory management of the whole system, the Linux kernel is the force behind the**

legendary Linux efficiency. The new edition of Understanding the Linux Kernel takes you on a guided tour through the most significant data structures, many algorithms, and programming tricks used in the kernel. Probing beyond the superficial features, the authors offer valuable insights to people who want to know how things really work inside their machine. Relevant segments of code are dissected and discussed line by line. The book covers more than just the functioning of the code, it explains the theoretical underpinnings for why Linux does things the way it does. The new edition of the book has been updated to cover version 2.4 of the kernel, which is quite different from version 2.2: the virtual memory system is entirely new, support for multiprocessor systems is improved, and whole new classes of hardware devices have been added. The authors explore each new feature in detail. Other topics in the book include: Memory management including file buffering, process swapping, and Direct memory Access (DMA) The Virtual Filesystem and the Second Extended Filesystem Process creation and scheduling Signals, interrupts, and the essential interfaces to device drivers Timing Synchronization in the kernel Interprocess Communication (IPC) Program execution Understanding the Linux Kernel, Second Edition will acquaint you with all the inner workings of Linux, but is more than just an academic exercise. You'll learn what conditions bring out Linux's best performance, and you'll see how it meets the challenge of providing good system response during process scheduling, file access, and memory management in a wide variety of environments. If knowledge is power, then this book will help you make the most of your Linux system.

PC HARDWARE IN A NUTSHELL

A DESKTOP QUICK REFERENCE

"*O'Reilly Media, Inc.*" **PC Hardware in a Nutshell is the practical guide to buying, building, upgrading, and repairing Intel-based PCs. A longtime favorite among PC users, the third edition of the book now contains useful information for people running either Windows or Linux operating systems. Written for novices and seasoned professionals alike, the book is packed with useful and unbiased information, including how-to advice for specific components, ample reference material, and a comprehensive case study on building a PC.In addition to coverage of the fundamentals and general tips about working on PCs, the book includes chapters focusing on motherboards, processors, memory, floppies, hard drives, optical drives, tape devices, video devices, input devices, audio components, communications, power supplies, and maintenance. Special emphasis is given to upgrading and troubleshooting existing equipment so you can get the most from your existing investments.This new edition is expanded to include: Detailed information about the latest motherboards and chipsets from AMD, Intel, SiS, and VIA Extensive coverage of the Pentium 4 and the**

latest AMD processors, including the Athlon XP/MP Full details about new hard drive standards, including the latest SCSI standards, ATA/133, Serial ATA, and the new 48-bit "Big Drive" ATA interface Extended coverage of DVD drives, including DVD-RAM, DVD-R/RW, and DVD+R/RW Details about Flat Panel Displays, including how to choose one (and why you might not want to) New chapters on serial communications, parallel communications, and USB communications (including USB 2.0) Enhanced troubleshooting coverage PC Hardware in a Nutshell, 3rd Edition provides independent, useful and practical information in a no-nonsense manner with specific recommendations on components. Based on real-world testing over time, it will help you make intelligent, informed decisions about buying, building, upgrading, and repairing PCs in a cost effective manner that will help you maximize new or existing computer hardware systems. It's loaded with real-world advice presented in a concise style that clearly delivers just the information you want, without your having to hunt for it.

ESSENTIALS OF COMPUTER ARCHITECTURE, SECOND EDITION

CRC Press **This easy to read textbook provides an introduction to computer architecture, while focusing on the essential aspects of hardware that programmers need to know. The topics are explained from a programmer’s point of view, and the text emphasizes consequences for programmers. Divided in five parts, the book covers the basics of digital logic, gates, and data paths, as well as the three primary aspects of architecture: processors, memories, and I/O systems. The book also covers advanced topics of parallelism, pipelining, power and energy, and performance. A hands-on lab is also included. The second edition contains three new chapters as well as changes and updates throughout.**

THE MEMORY SYSTEM

YOU CAN'T AVOID IT, YOU CAN'T IGNORE IT, YOU CAN'T FAKE IT

Morgan & Claypool Publishers **Today, computer-system optimization, at both the hardware and software levels, must consider the details of the memory system in its analysis; failing to do so yields systems that are increasingly inefficient as those systems become more complex. This lecture seeks to introduce the reader to the most important details of the memory system; it targets both computer scientists and computer engineers in industry and in academia. Roughly speaking, computer scientists are the users of the memory system and computer engineers are the designers of the memory system. Both can benefit tremendously from a basic understanding of how the memory system really works: the computer scientist will be better equipped to create algorithms that perform well and the**

computer engineer will be better equipped to design systems that approach the optimal, given the resource limitations. Currently, there is consensus among architecture researchers that the memory system is "the bottleneck," and this consensus has held for over a decade. Somewhat inexplicably, most of the research in the field is still directed toward improving the CPU to better tolerate a slow memory system, as opposed to addressing the weaknesses of the memory system directly. This lecture should get the bulk of the computer science and computer engineering population up the steep part of the learning curve. Not every CS/CE researcher/developer needs to do work in the memory system, but, just as a carpenter can do his job more efficiently if he knows a little of architecture, and an architect can do his job more efficiently if he knows a little of carpentry, giving the CS/CE worlds better intuition about the memory system should help them build better systems, both software and hardware. Table of Contents: Primers / It Must Be Modeled Accurately / ...\ and It Will Change Soon

PERFORMANCE ANALYSIS AND TUNING FOR GENERAL PURPOSE GRAPHICS PROCESSING UNITS (GPGPU)

Morgan & Claypool Publishers **General-purpose graphics processing units (GPGPU) have emerged as an important class of shared memory parallel processing architectures, with widespread deployment in every computer class from high-end supercomputers to embedded mobile platforms. Relative to more traditional multicore systems of today, GPGPUs have distinctly higher degrees of hardware multithreading (hundreds of hardware thread contexts vs. tens), a return to wide vector units (several tens vs. 1-10), memory architectures that deliver higher peak memory bandwidth (hundreds of gigabytes per second vs. tens), and smaller caches/scratchpad memories (less than 1 megabyte vs. 1-10 megabytes).In this book, we provide a high-level overview of current GPGPU architectures and programming models. We review the principles that are used in previous shared memory parallel platforms, focusing on recent results in both the theory and practice of parallel algorithms, and suggest a connection to GPGPU platforms. We aim to provide hints to architects about understanding algorithm aspect to GPGPU. We also provide detailed performance analysis and guide optimizations from high-level algorithms to low-level instruction level optimizations. As a case study, we use n-body particle simulations known as the fast multipole method (FMM) as an example. We also briefly survey the state-of-the-art in GPU performance analysis tools and techniques.**

SHARED-MEMORY SYNCHRONIZATION

Springer Nature **From driving, flying, and swimming, to digging for unknown objects in space exploration, autonomous**

robots take on varied shapes and sizes. In part, autonomous robots are designed to perform tasks that are too dirty, dull, or dangerous for humans. With nontrivial autonomy and volition, they may soon claim their own place in human society. These robots will be our allies as we strive for understanding our natural and man-made environments and build positive synergies around us. Although we may never perfect replication of biological capabilities in robots, we must harness the inevitable emergence of robots that synchronizes with our own capacities to live, learn, and grow. This book is a snapshot of motivations and methodologies for our collective attempts to transform our lives and enable us to cohabit with robots that work with and for us. It reviews and guides the reader to seminal and continual developments that are the foundations for successful paradigms. It attempts to demystify the abilities and limitations of robots. It is a progress report on the continuing work that will fuel future endeavors. Table of Contents: Part I: Preliminaries/Agency, Motion, and Anatomy/Behaviors / Architectures / Affect/Sensors / Manipulators/Part II: Mobility/Potential Fields/Roadmaps / Reactive Navigation / Multi-Robot Mapping: Brick and Mortar Strategy / Part III: State of the Art / Multi-Robotics Phenomena / Human-Robot Interaction / Fuzzy Control / Decision Theory and Game Theory / Part IV: On the Horizon / Applications: Macro and Micro Robots / References / Author Biography / Discussion

SEE MIPS RUN

Elsevier **See MIPS Run, Second Edition, is not only a thorough update of the first edition, it is also a marriage of the best-known RISC architecture--MIPS--with the best-known open-source OS--Linux. The first part of the book begins with MIPS design principles and then describes the MIPS instruction set and programmers' resources. It uses the MIPS32 standard as a baseline (the 1st edition used the R3000) from which to compare all other versions of the architecture and assumes that MIPS64 is the main option. The second part is a significant change from the first edition. It provides concrete examples of operating system low level code, by using Linux as the example operating system. It describes how Linux is built on the foundations the MIPS hardware provides and summarizes the Linux application environment, describing the libraries, kernel device-drivers and CPU-specific code. It then digs deep into application code and library support, protection and memory management, interrupts in the Linux kernel and multiprocessor Linux. Sweetman has revised his best-selling MIPS bible for MIPS programmers, embedded systems designers, developers and programmers, who need an in-depth understanding of the MIPS architecture and specific guidance for writing software for MIPS-based systems, which are increasingly Linux-based. Completely new material offers the best explanation available on how Linux runs on real hardware. Provides a complete, updated and easy-to-use guide to the MIPS instruction set using the MIPS32 standard as the baseline architecture with the MIPS64 as the main option. Retains the same**

engaging writing style that made the first edition so readable, reflecting the authors 20+ years experience in designing systems based on the MIPS architecture.

PROGRAMMING PERSISTENT MEMORY

A COMPREHENSIVE GUIDE FOR DEVELOPERS

Apress **Beginning and experienced programmers will use this comprehensive guide to persistent memory programming. You will understand how persistent memory brings together several new software/hardware requirements, and offers great promise for better performance and faster application startup times—a huge leap forward in byte-addressable capacity compared with current DRAM offerings. This revolutionary new technology gives applications significant performance and capacity improvements over existing technologies. It requires a new way of thinking and developing, which makes this highly disruptive to the IT/computing industry. The full spectrum of industry sectors that will benefit from this technology include, but are not limited to, in-memory and traditional databases, AI, analytics, HPC, virtualization, and big data. Programming Persistent Memory describes the technology and why it is exciting the industry. It covers the operating system and hardware requirements as well as how to create development environments using emulated or real persistent memory hardware. The book explains fundamental concepts; provides an introduction to persistent memory programming APIs for C, C++, JavaScript, and other languages; discusses RMDA with persistent memory; reviews security features; and presents many examples. Source code and examples that you can run on your own systems are included. What You'll Learn Understand what persistent memory is, what it does, and the value it brings to the industry Become familiar with the operating system and hardware requirements to use persistent memory Know the fundamentals of persistent memory programming: why it is different from current programming methods, and what developers need to keep in mind when programming for persistence Look at persistent memory application development by example using the Persistent Memory Development Kit (PMDK)Design and optimize data structures for persistent memoryStudy how real-world applications are modified to leverage persistent memoryUtilize the tools available for persistent memory programming, application performance profiling, and debugging Who This Book Is For C, C++, Java, and Python developers, but will also be useful to software, cloud, and hardware architects across a broad spectrum of sectors, including cloud service providers, independent software vendors, high performance compute, artificial intelligence, data analytics, big data, etc.**

EURO-PAR 2003 PARALLEL PROCESSING

9TH INTERNATIONAL EURO-PAR CONFERENCE, KLAGENFURT, AUSTRIA, AUGUST 26–29, 2003 PROCEEDINGS

Springer **Euro-ParConferenceSeries The European Conference on Parallel Computing (Euro-Par) is an international conference series dedicated to the promotion and advancement of all aspects of parallel and distributed computing. The major themes fall into the categories of hardware, software, algorithms, and applications. This year, new and interesting topicswereintroduced,likePeer-to-PeerComputing,DistributedMultimedia- stems, and Mobile and Ubiquitous Computing. For the ?rst time, we organized a Demo Session showing many challenging applications. The general objective of Euro-Par is to provide a forum promoting the de- lopment of parallel and distributed computing both as an industrial technique and an academic discipline, extending the frontiers of both the state of the art and the state of the practice. The industrial importance of parallel and dist- buted computing is supported this year by a special Industrial Session as well as a vendors' exhibition. This is particularly important as currently parallel and distributed computing is evolving into a globally important technology; the b- zword Grid Computing clearly expresses this move. In addition, the trend to a - bile world is clearly visible in this year's Euro-Par. ThemainaudienceforandparticipantsatEuro-Parareresearchersinaca- mic departments, industrial organizations, and government laboratories. Euro- Par aims to become the primary choice of such professionals for the presentation of new results in their speci?c areas. Euro-Par has its own Internet domain with a permanent Web site where the history of the conference series is described: http://www.euro-par.org. The Euro-Par conference series is sponsored by the Association for Computer Machinery (ACM) and the International Federation for Information Processing (IFIP).**

COMPUTER ARCHITECTURE

A QUANTITATIVE APPROACH

Elsevier **The era of seemingly unlimited growth in processor performance is over: single chip architectures can no longer overcome the performance limitations imposed by the power they consume and the heat they generate. Today, Intel and other semiconductor firms are abandoning the single fast processor model in favor of multi-core microprocessors--chips that combine two or more processors in a single package. In the fourth edition of Computer Architecture, the authors focus on this historic shift, increasing their coverage of multiprocessors and exploring the**

most effective ways of achieving parallelism as the key to unlocking the power of multiple processor architectures. Additionally, the new edition has expanded and updated coverage of design topics beyond processor performance, including power, reliability, availability, and dependability. CD System Requirements PDF Viewer The CD material includes PDF documents that you can read with a PDF viewer such as Adobe, Acrobat or Adobe Reader. Recent versions of Adobe Reader for some platforms are included on the CD. HTML Browser The navigation framework on this CD is delivered in HTML and JavaScript. It is recommended that you install the latest version of your favorite HTML browser to view this CD. The content has been verified under Windows XP with the following browsers: Internet Explorer 6.0, Firefox 1.5; under Mac OS X (Panther) with the following browsers: Internet Explorer 5.2, Firefox 1.0.6, Safari 1.3; and under Mandriva Linux 2006 with the following browsers: Firefox 1.0.6, Konqueror 3.4.2, Mozilla 1.7.11. The content is designed to be viewed in a browser window that is at least 720 pixels wide. You may find the content does not display well if your display is not set to at least 1024x768 pixel resolution. Operating System This CD can be used under any operating system that includes an HTML browser and a PDF viewer. This includes Windows, Mac OS, and most Linux and Unix systems. Increased coverage on achieving parallelism with multiprocessors. Case studies of latest technology from industry including the Sun Niagara Multiprocessor, AMD Opteron, and Pentium 4. Three review appendices, included in the printed volume, review the basic and intermediate principles the main text relies upon. Eight reference appendices, collected on the CD, cover a range of topics including specific architectures, embedded systems, application specific processors--some guest authored by subject experts.

COMPUTER ORGANIZATION AND DESIGN RISC-V EDITION

THE HARDWARE SOFTWARE INTERFACE

Morgan Kaufmann **The new RISC-V Edition of Computer Organization and Design features the RISC-V open source instruction set architecture, the first open source architecture designed to be used in modern computing environments such as cloud computing, mobile devices, and other embedded systems. With the post-PC era now upon us, Computer Organization and Design moves forward to explore this generational change with examples, exercises, and material highlighting the emergence of mobile computing and the Cloud. Updated content featuring tablet computers, Cloud infrastructure, and the x86 (cloud computing) and ARM (mobile computing devices) architectures is included. An online companion Web site provides advanced content for further study, appendices, glossary, references, and recommended reading. Features RISC-V, the first such architecture designed to be used in modern computing environments, such as**

cloud computing, mobile devices, and other embedded systems Includes relevant examples, exercises, and material highlighting the emergence of mobile computing and the cloud

APPLIED PARALLEL COMPUTING: ADVANCED SCIENTIFIC COMPUTING

6TH INTERNATIONAL CONFERENCE, PARA 2002, ESPOO, FINLAND, JUNE 15-18, 2002. PROCEEDINGS

Springer **This book constitutes the refereed proceedings of the 6th International Conference on Applied Parallel Computing, PARA 2002, held in Espoo, Finland, in June 2002. The 50 revised full papers presented together with nine keynote lectures were carefully reviewed and selected for inclusion in the proceedings. The papers are organized in topical sections on data mining and knowledge discovery, parallel program development, practical experience in parallel computing, computer science, numerical algorithms with hierarchical memory optimization, numerical methods and algorithms, cluster computing, grid and network technologies, and physics and applications.**

INTRODUCTION TO EMBEDDED SYSTEMS

A CYBER-PHYSICAL SYSTEMS APPROACH

MIT Press **An introduction to the engineering principles of embedded systems, with a focus on modeling, design, and analysis of cyber-physical systems. The most visible use of computers and software is processing information for human consumption. The vast majority of computers in use, however, are much less visible. They run the engine, brakes, seatbelts, airbag, and audio system in your car. They digitally encode your voice and construct a radio signal to send it from your cell phone to a base station. They command robots on a factory floor, power generation in a power plant, processes in a chemical plant, and traffic lights in a city. These less visible computers are called embedded systems, and the software they run is called embedded software. The principal challenges in designing and analyzing embedded systems stem from their interaction with physical processes. This book takes a cyber-physical approach to embedded systems, introducing the engineering concepts underlying embedded systems as a technology and as a subject of study. The focus is on modeling, design, and analysis of cyber-physical systems, which integrate computation, networking, and physical processes. The second edition offers two new chapters, several new exercises, and other improvements. The book can be used as a textbook at the advanced undergraduate or introductory graduate level and as a professional reference for practicing engineers and computer scientists. Readers should have some**

familiarity with machine structures, computer programming, basic discrete mathematics and algorithms, and signals and systems.

ARM SYSTEM DEVELOPER'S GUIDE

DESIGNING AND OPTIMIZING SYSTEM SOFTWARE

Elsevier **Over the last ten years, the ARM architecture has become one of the most pervasive architectures in the world, with more than 2 billion ARM-based processors embedded in products ranging from cell phones to automotive braking systems. A world-wide community of ARM developers in semiconductor and product design companies includes software developers, system designers and hardware engineers. To date no book has directly addressed their need to develop the system and software for an ARM-based system. This text fills that gap. This book provides a comprehensive description of the operation of the ARM core from a developer’s perspective with a clear emphasis on software. It demonstrates not only how to write efficient ARM software in C and assembly but also how to optimize code. Example code throughout the book can be integrated into commercial products or used as templates to enable quick creation of productive software. The book covers both the ARM and Thumb instruction sets, covers Intel's XScale Processors, outlines distinctions among the versions of the ARM architecture, demonstrates how to implement DSP algorithms, explains exception and interrupt handling, describes the cache technologies that surround the ARM cores as well as the most efficient memory management techniques. A final chapter looks forward to the future of the ARM architecture considering ARMv6, the latest change to the instruction set, which has been designed to improve the DSP and media processing capabilities of the architecture. * No other book describes the ARM core from a system and software perspective. * Author team combines extensive ARM software engineering experience with an in-depth knowledge of ARM developer needs. * Practical, executable code is fully explained in the book and available on the publisher's Website. * Includes a simple embedded operating system.**

DIGITAL DESIGN AND COMPUTER ARCHITECTURE

ARM EDITION

Morgan Kaufmann **Digital Design and Computer Architecture: ARM Edition covers the fundamentals of digital logic design and reinforces logic concepts through the design of an ARM microprocessor. Combining an engaging and humorous**

writing style with an updated and hands-on approach to digital design, this book takes the reader from the fundamentals of digital logic to the actual design of an ARM processor. By the end of this book, readers will be able to build their own microprocessor and will have a top-to-bottom understanding of how it works. Beginning with digital logic gates and progressing to the design of combinational and sequential circuits, this book uses these fundamental building blocks as the basis for designing an ARM processor. SystemVerilog and VHDL are integrated throughout the text in examples illustrating the methods and techniques for CAD-based circuit design. The companion website includes a chapter on I/O systems with practical examples that show how to use the Raspberry Pi computer to communicate with peripheral devices such as LCDs, Bluetooth radios, and motors. This book will be a valuable resource for students taking a course that combines digital logic and computer architecture or students taking a two-quarter sequence in digital logic and computer organization/architecture. Covers the fundamentals of digital logic design and reinforces logic concepts through the design of an ARM microprocessor. Features side-by-side examples of the two most prominent Hardware Description Languages (HDLs)—SystemVerilog and VHDL—which illustrate and compare the ways each can be used in the design of digital systems. Includes examples throughout the text that enhance the reader's understanding and retention of key concepts and techniques. The Companion website includes a chapter on I/O systems with practical examples that show how to use the Raspberry Pi computer to communicate with peripheral devices such as LCDs, Bluetooth radios, and motors. The Companion website also includes appendices covering practical digital design issues and C programming as well as links to CAD tools, lecture slides, laboratory projects, and solutions to exercises.

THE MATRIX EIGENVALUE PROBLEM

GR AND KRYLOV SUBSPACE METHODS

SIAM **The first in-depth, complete, and unified theoretical discussion of the two most important classes of algorithms for solving matrix eigenvalue problems: QR-like algorithms for dense problems and Krylov subspace methods for sparse problems. The author discusses the theory of the generic GR algorithm, including special cases (for example, QR, SR, HR), and the development of Krylov subspace methods. This book also addresses a generic Krylov process and the Arnoldi and various Lanczos algorithms, which are obtained as special cases. Theoretical and computational exercises guide students, step by step, to the results. Downloadable MATLAB programs, compiled by the author, are available on a supplementary Web site. Readers of this book are expected to be familiar with the basic ideas of linear**

algebra and to have had some experience with matrix computations. Ideal for graduate students, or as a reference book for researchers and users of eigenvalue codes.

SERVER ARCHITECTURES

MULTIPROCESSORS, CLUSTERS, PARALLEL SYSTEMS, WEB SERVERS, STORAGE SOLUTIONS

Elsevier **The goal of this book is to present and compare various options one for systems architecture from two separate points of view. One, that of the information technology decision-maker who must choose a solution matching company business requirements, and secondly that of the systems architect who finds himself between the rock of changes in hardware and software technologies and the hard place of changing business needs. Different aspects of server architecture are presented, from databases designed for parallel architectures to high-availability systems, and touching en route on often- neglected performance aspects. The book provides IT managers, decision makers and project leaders who want to acquire knowledge sufficient to understand the choices made in and capabilities of systems offered by various vendors Provides system design information to balance the characteristic applications against the capabilities and nature of various architectural choices In addition, it offers an integrated view of the concepts in server architecture, accompanied by discussion of effects on the evolution of the data processing industry**

DISTRIBUTED ALGORITHMS, SECOND EDITION

AN INTUITIVE APPROACH

MIT Press **The new edition of a guide to distributed algorithms that emphasizes examples and exercises rather than the intricacies of mathematical models. This book offers students and researchers a guide to distributed algorithms that emphasizes examples and exercises rather than the intricacies of mathematical models. It avoids mathematical argumentation, often a stumbling block for students, teaching algorithmic thought rather than proofs and logic. This approach allows the student to learn a large number of algorithms within a relatively short span of time. Algorithms are explained through brief, informal descriptions, illuminating examples, and practical exercises. The examples and exercises allow readers to understand algorithms intuitively and from different perspectives. Proof sketches, arguing the correctness of an algorithm or explaining the idea behind fundamental results, are also included. The algorithms presented in the book are for the most part “classics,” selected because they shed light on the algorithmic design of**

distributed systems or on key issues in distributed computing and concurrent programming. This second edition has been substantially revised. A new chapter on distributed transaction offers up-to-date treatment of database transactions and the important evolving area of transactional memory. A new chapter on security discusses two exciting new topics: blockchains and quantum cryptography. Sections have been added that cover such subjects as rollback recovery, fault-tolerant termination detection, and consensus for shared memory. An appendix offers pseudocode descriptions of many algorithms. Solutions and slides are available for instructors. Distributed Algorithms can be used in courses for upper-level undergraduates or graduate students in computer science, or as a reference for researchers in the field.

INSIDE THE MACHINE

AN ILLUSTRATED INTRODUCTION TO MICROPROCESSORS AND COMPUTER ARCHITECTURE

No Starch Press **Om hvordan mikroprocessorer fungerer, med undersøgelse af de nyeste mikroprocessorer fra Intel, IBM og Motorola.**

LEARNING APACHE CASSANDRA

Packt Publishing Ltd **Build a scalable, fault-tolerant and highly available data layer for your applications using Apache Cassandra About This Book Install Cassandra and set up multi-node clusters Design rich schemas that capture the relationships between different data types Master the advanced features available in Cassandra 3.x through a step-by-step tutorial and build a scalable, high performance database layer Who This Book Is For If you are a NoSQL developer and new to Apache Cassandra who wants to learn its common as well as not-so-common features, this book is for you. Alternatively, a developer wanting to enter the world of NoSQL will find this book useful. It does not assume any prior experience in coding or any framework. What You Will Learn Install Cassandra Create keyspaces and tables with multiple clustering columns to organize related data Use secondary indexes and materialized views to avoid denormalization of data Effortlessly handle concurrent updates with collection columns Ensure data integrity with lightweight transactions and logged batches Understand eventual consistency and use the right consistency level for your situation Understand data distribution with Cassandra Develop simple application using Java driver and implement application-level optimizations In Detail Cassandra is a distributed database that stands out thanks to its robust feature set and intuitive interface, while providing high availability and scalability of a distributed data store.**

This book will introduce you to the rich feature set offered by Cassandra, and empower you to create and manage a highly scalable, performant and fault-tolerant database layer. The book starts by explaining the new features implemented in Cassandra 3.x and get you set up with Cassandra. Then you'll walk through data modeling in Cassandra and the rich feature set available to design a flexible schema. Next you'll learn to create tables with composite partition keys, collections and user-defined types and get to know different methods to avoid denormalization of data. You will then proceed to create user-defined functions and aggregates in Cassandra. Then, you will set up a multi node cluster and see how the dynamics of Cassandra change with it. Finally, you will implement some application-level optimizations using a Java client. By the end of this book, you'll be fully equipped to build powerful, scalable Cassandra database layers for your applications. Style and approach This book takes a step-by- step approach to give you basic to intermediate knowledge of Apache Cassandra. Every concept is explained in depth, and is supplemented with practical examples when required.

COMPUTER ARCHITECTURE

A QUANTITATIVE APPROACH

Morgan Kaufmann Pub **"Once in a great while, a landmark computer-science book is published. Computer Architecture: A Quantitative Approach, Second Edition, is such a book. In an era of fluff computer books that are, quite properly, remaindered within weeks of publication, this book will stand the test of time, becoming lovingly dog-eared in the hands of anyone who designs computers or has concerns about the performance of computer programs. " - Robert Bernecky, Dr. Dobb's Journal , April 1998 Computer Architecture: A Quantitative Approach was the first book to focus on computer architecture as a modern science. Its publication in 1990 inspired a new approach to studying and understanding computer design. Now, the second edition explores the next generation of architectures and design techniques with view to the future. A basis for modern computer architecture As the authors explain in their preface to the Second Edition, computer architecture itself has undergone significant change since 1990. Concentrating on currently predominant and emerging commercial systems, the Hennessy and Patterson have prepared entirely new chapters covering additional advanced topics:* Advanced Pipelining: A new chapter emphasizes superscalar and multiple issues.* Networks: A new chapter examines in depth the design issues for small and large shared-memory multiprocessors.* Storage Systems: Expanded presentation includes coverage of I/O performance measures.* Memory: Expanded coverage of caches and memory-hierarchy design addresses contemporary design issues.* Examples and**

Exercises: Completely revised on current architectures such as MIPS R4000, Intel 80x86 and Pentium, PowerPC, and HP PA-RISC. Distinctive presentation This book continues the style of the first edition, with revised sections on Fallacies and Pitfalls, Putting It All Together and Historical Perspective, and contains entirely new sections on Crosscutting Issues. The focus on fundamental techniques for designing real machines and the attention to maximizing cost/performance are crucial to both students and working professionals. Anyone involved in building computers, from palmtops to supercomputers, will profit from the expertise offered by Hennessy and Patterson.

COMPUTER ORGANIZATION & ARCHITECTURE 7E

Pearson Education India

LINUX DEVICE DRIVERS

"*O'Reilly Media, Inc.*" **Provides information on writing a driver in Linux, covering such topics as character devices, network interfaces, driver debugging, concurrency, and interrupts.**

AN INTRODUCTION TO PARALLEL PROGRAMMING

Morgan Kaufmann **An Introduction to Parallel Programming, Second Edition presents a tried-and-true tutorial approach that shows students how to develop effective parallel programs with MPI, Pthreads and OpenMP. As the first undergraduate text to directly address compiling and running parallel programs on multi-core and cluster architecture, this second edition carries forward its clear explanations for designing, debugging and evaluating the performance of distributed and shared-memory programs while adding coverage of accelerators via new content on GPU programming and heterogeneous programming. New and improved user-friendly exercises teach students how to compile, run and modify example programs. Takes a tutorial approach, starting with small programming examples and building progressively to more challenging examples Explains how to develop parallel programs using MPI, Pthreads and OpenMP programming models A robust package of online ancillaries for instructors and students includes lecture slides, solutions manual, downloadable source code, and an image bank New to this edition: New chapters on GPU programming and heterogeneous programming New examples and exercises related to parallel algorithms**

ENGINEERING A COMPILER

Elsevier **This entirely revised second edition of Engineering a Compiler is full of technical updates and new material covering the latest developments in compiler technology. In this comprehensive text you will learn important techniques for constructing a modern compiler. Leading educators and researchers Keith Cooper and Linda Torczon combine basic principles with pragmatic insights from their experience building state-of-the-art compilers. They will help you fully understand important techniques such as compilation of imperative and object-oriented languages, construction of static single assignment forms, instruction scheduling, and graph-coloring register allocation. In-depth treatment of algorithms and techniques used in the front end of a modern compiler Focus on code optimization and code generation, the primary areas of recent research and development Improvements in presentation including conceptual overviews for each chapter, summaries and review questions for sections, and prominent placement of definitions for new terms Examples drawn from several different programming languages**

HIGH PERFORMANCE PYTHON

PRACTICAL PERFORMANT PROGRAMMING FOR HUMANS

"*O'Reilly Media, Inc.*" **Your Python code may run correctly, but you need it to run faster. Updated for Python 3, this expanded edition shows you how to locate performance bottlenecks and significantly speed up your code in high-data-volume programs. By exploring the fundamental theory behind design choices, High Performance Python helps you gain a deeper understanding of Python’s implementation. How do you take advantage of multicore architectures or clusters? Or build a system that scales up and down without losing reliability? Experienced Python programmers will learn concrete solutions to many issues, along with war stories from companies that use high-performance Python for social media analytics, productionized machine learning, and more. Get a better grasp of NumPy, Cython, and profilers Learn how Python abstracts the underlying computer architecture Use profiling to find bottlenecks in CPU time and memory usage Write efficient programs by choosing appropriate data structures Speed up matrix and vector computations Use tools to compile Python down to machine code Manage multiple I/O and computational operations concurrently Convert multiprocessing code to run on local or remote clusters Deploy code faster using tools like Docker**

MODERN COMPILER IMPLEMENTATION IN C

Cambridge University Press **This new, expanded textbook describes all phases of a modern compiler: lexical analysis, parsing, abstract syntax, semantic actions, intermediate representations, instruction selection via tree matching, dataflow analysis, graph-coloring register allocation, and runtime systems. It includes good coverage of current techniques in code generation and register allocation, as well as functional and object-oriented languages, that are missing from most books. In addition, more advanced chapters are now included so that it can be used as the basis for a two-semester or graduate course. The most accepted and successful techniques are described in a concise way, rather than as an exhaustive catalog of every possible variant. Detailed descriptions of the interfaces between modules of a compiler are illustrated with actual C header files. The first part of the book, Fundamentals of Compilation, is suitable for a one-semester first course in compiler design. The second part, Advanced Topics, which includes the advanced chapters, covers the compilation of object-oriented and functional languages, garbage collection, loop optimizations, SSA form, loop scheduling, and optimization for cache-memory hierarchies.**

THE ART OF MEMORY FORENSICS

DETECTING MALWARE AND THREATS IN WINDOWS, LINUX, AND MAC MEMORY

John Wiley & Sons **Memory forensics provides cutting edge technology to help investigate digital attacks Memory forensics is the art of analyzing computer memory (RAM) to solve digital crimes. As a follow-up to the best seller Malware Analyst's Cookbook, experts in the fields of malware, security, and digital forensics bring you a step-by-step guide to memory forensics—now the most sought after skill in the digital forensics and incident response fields. Beginning with introductory concepts and moving toward the advanced, The Art of Memory Forensics: Detecting Malware and Threats in Windows, Linux, and Mac Memory is based on a five day training course that the authors have presented to hundreds of students. It is the only book on the market that focuses exclusively on memory forensics and how to deploy such techniques properly. Discover memory forensics techniques: How volatile memory analysis improves digital investigations Proper investigative steps for detecting stealth malware and advanced threats How to use free, open source tools for conducting thorough memory forensics Ways to acquire memory from suspect systems in a forensically sound manner The next era of malware and security breaches are more sophisticated and targeted, and the volatile memory of a computer is often overlooked or destroyed as part of the incident response process. The**

Art of Memory Forensics explains the latest technological innovations in digital forensics to help bridge this gap. It covers the most popular and recently released versions of Windows, Linux, and Mac, including both the 32 and 64-bit editions.

DRAM CIRCUIT DESIGN

FUNDAMENTAL AND HIGH-SPEED TOPICS

John Wiley & Sons **A modern, comprehensive introduction to DRAM for students and practicing chip designers Dynamic Random Access Memory (DRAM) technology has been one of the greatestdriving forces in the advancement of solid-state technology. With its ability to produce high product volumes and low pricing, it forces solid-state memory manufacturers to work aggressively to cut costs while maintaining, if not increasing, their market share. As a result, the state of the art continues to advance owing to the tremendous pressure to get more memory chips from each silicon wafer, primarily through process scaling and clever design. From a team of engineers working in memory circuit design, DRAM Circuit Design gives students and practicing chip designers an easy-to-follow, yet thorough, introductory treatment of the subject. Focusing on the chip designer rather than the end user, this volume offers expanded, up-to-date coverage of DRAM circuit design by presenting both standard and high-speed implementations. Additionally, it explores a range of topics: the DRAM array, peripheral circuitry, global circuitry and considerations, voltage converters, synchronization in DRAMs, data path design, and power delivery. Additionally, this up-to-date and comprehensive book features topics in high-speed design and architecture and the ever-increasing speed requirements of memory circuits. The only book that covers the breadth and scope of the subject under one cover, DRAM Circuit Design is an invaluable introduction for students in courses on memory circuit design or advanced digital courses in VLSI or CMOS circuit design. It also serves as an essential, one-stop resource for academics, researchers, and practicing engineers.**